

**WHAT IS CLAIMED IS:**

1. A single-chip audio system comprising:  
a bus interface;  
digital to analog converters for converting digital  
5 audio data received through said bus to analog signals;  
an analog mixer for mixing signals received from  
said digital to analog converters with an analog signal  
received from an external source; and  
analog spacial enhancement circuitry for enhancing  
10 first and second mixed analog signals output from said  
analog mixer.
2. The system of Claim 1 wherein said digital to analog  
converters comprise:  
first selectable digital to analog converters for  
15 selectably converting higher sound quality digital  
signals; and  
second selectable digital to analog converters for  
selectively converting lower sound quality digital  
signals.
- 20 3. The system of Claim 2 wherein said higher quality  
sound digital signals are received through said bus  
interface.
4. The audio system of Claim 3 wherein said bus  
interface interfaces with an ISA.
- 25 5. The system of Claim 2 wherein said lower quality  
sound digital signals are received by said second digital  
to analog converters from an on chip FM synthesizer.

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6. The system of Claim 2 wherein said lower quality sound digital signals are received by said second digital to analog converters from an external wavetable device.

- 5 7. The system of Claim 1 wherein said analog spatial enhancement circuitry comprises:
- a difference amplifier for generating a difference signal from said first and second signals output from said mixer;
  - a filter for generating an acoustic crosstalk compensation signal from said difference signal;
  - an inverter for inverting said compensation signal;
  - a first summer for summing said inverted compensation signal with said first signal; and
  - a second summer for summing said compensation signal with said second signal.
- 10 8. The system of Claim 1 and further comprising:
- mute controls for muting said signals received said mixer; and
  - circuitry for idling said digital to analog converters when said muting controls are asserted.
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9. The system of Claim 8 and further comprising circuitry for idling said mixer when said mute controls are asserted.

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10. Audio spatial enhancement circuitry comprising:  
circuitry for generating a difference signal from  
left and right channel analog data streams;  
circuitry for generating an acoustic crosstalk  
5 compensation signal;  
circuitry for summing said left channel data stream  
with said compensation signal; and  
circuitry for summing said right channel data stream  
with an inverted said compensation signal.
- 10 11. The audio spatial enhancement circuitry of Claim 10  
wherein said circuitry for generating a compensation  
signal comprises a filter.
12. The audio spatial enhancement circuitry of Claim 11  
wherein said filter comprises a notch filter.
- 15 13. The audio spatial enhancement circuitry of Claim 11  
wherein said filter comprises an active filter.
14. The audio spatial enhancement circuitry of Claim 10  
wherein said circuitry for generating a difference signal  
comprises a difference amplifier.
- 20 15. The audio spatial enhancement circuitry of Claim 10  
wherein said circuitry for summing said left channel data  
stream with said compensation signal comprises an analog  
summer.
- 25 16. The audio spatial enhancement circuitry of Claim 15  
wherein said analog summer has a gain of one-half.

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17. The audio spatial enhancement circuitry of Claim 10 wherein said circuitry for summing said right channel data stream and said inverted compensation signal comprises an analog summer and an analog inverter.
- 5 18. The audio spatial enhancement circuitry of Claim 17 wherein said analog summer has a gain of one.

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19. An audio system comprising:

digital to analog converters having left and right paths for converting received left and right streams of audio data;

5 a plurality of analog data ports for receiving left and right channel streams of audio data;

a mixer having left and right paths for selectively mixing respective left and right channel data passed from said converters and left and right channel data passed from said ports;

10 muting circuitry for selectively muting said right and left channel data to be passed to said mixer from said converters; and

15 circuitry for idling a selected one of said left and right paths of said mixer when selected data passed to said mixer is muted.

20. The system of Claim 19 wherein said left path of said mixer is idled when selected left channel data passed to said mixer is muted.

21. The system of Claim 19 wherein a selected left channel data port is idled when selected left channel data passed to said mixer is muted.

22. The system of Claim 19 wherein said left path of said converters is idled when selected left channel data passed to said mixer is muted.

23. The system of Claim 19 wherein said right path of said mixer is idled when selected right channel data passed to said mixer is muted.

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24. The system of Claim 19 wherein a selected right channel data port is idled when selected right channel data passed to said mixer is muted.

- 5 25. The system of Claim 19 wherein said right path of said converters is idled when selected right channel data passed to said mixer is muted.

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26. Amplitude control circuitry comprising:

a first register for storing received amplitude control data;

5 a second register for storing amplitude control data transferred from said first register;

output circuitry for controlling the amplitude of a received signal in response to amplitude data transferred from said second register;

10 a sensor for determining when data stored in said first and second registers does not match; and

15 a comparator enabled by said sensor when said data in said first and second registers does not match, said comparator comparing a signal output from said output circuitry with a reference signal, and generating a signal for enabling the transfer of data from said first register to said second register when said signal output from said output circuitry falls within a window defined by said reference voltage.

27. The circuitry of Claim 26 wherein said received signal comprises an analog audio signal.

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28. The circuitry of Claim wherein said output circuitry comprises:

a decoder for decoding amplitude control data from said second register; and

5 an attenuator for attenuating said received signal in response to an output of the decoder.

29. The circuitry of Claim 28 wherein said decoder comprises a plurality of resistor taps and said decoder selects a selected one of said taps to provide selected attenuation to said received signal.

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30. The circuitry of Claim 28 wherein said output circuitry further comprises an operational amplifier for driving signals output from said output circuitry.

31. The circuitry of Claim 28 and further comprising a timer, said timer enabling the transfer of data from said first to said second register a preselected number of clock cycles after said sensor detects a mismatch between the contents of the first register and the contents of the second register.

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32. An audio system comprising:

circuitry for generating an audio data stream;  
circuitry for generating digital words defining a  
volume control level; and

5 volume control circuitry for controlling the  
amplitude of said audio data stream in response to said  
digital words comprising:

a master register for holding digital words  
received from said circuitry for generating;

10 a slave register for holding digital words  
selectively transferred from said master register in  
response to an enable signal;

output control circuitry for receiving said  
audio data stream and applying a preselected gain  
15 defined by a said digital word held in said slave  
register; and

circuitry for generating said enable signal  
when a said digital word held in said master  
register changes and said audio data stream output  
20 from said output control circuitry reaches a  
zero-crossing.

33. The audio system of Claim 32 wherein said output  
control circuitry applies a positive gain.

34. The audio system of Claim 32 wherein said output  
25 control circuitry applies a negative gain.

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35. The audio system of Claim 32 wherein said output control circuitry comprises:

a decoder for decoding a said digital word stored in said slave register; and

5 gain control circuitry for receiving said audio data stream at a first volume level and outputting said audio at a second volume level in responses to an output of the decoder.

10 36. The audio system of Claim 35 wherein said gain control circuitry comprises an attenuator.

37. The audio system of Claim 32 wherein said circuitry for generating digital data words and said volume control circuitry are disposed on a single integrated circuit chip.

15 38. The audio system of Claim 32 wherein said circuitry for generating an enable signal comprises:

a sensor for determining when first data stored in said master register does not match second data stored in said slave register; and

20 a comparator for comparing said stream output from said output circuitry against a predetermined reference when said first and second data do not match.

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39. An audio system disposed on a single chip:

an output mixer having inputs for receiving first  
digital audio data of a first bitwidth from a first  
digital to analog converter, second digital audio data  
of a second bitwidth from a second digital to analog  
converter, and analog data from an external source;

an output port for driving an analog signal output  
from said output mixer;

an input mixer having inputs for receiving analog  
data from a plurality of sources;

analog to digital converters for converting an  
analog output of said input mixer into digital data; and

an input path for transmitting said digital data  
output from said analog to digital converters to an  
external digital bus.

40. The audio system of Claim 39 wherein said first  
digital audio data is input to said first digital to  
analog converter from said external bus.

41. The audio system of Claim 39 and further comprising  
an FM synthesizer, said synthesizer outputting data to an  
input of said second digital to analog converter.

42. The audio system of Claim 39 wherein an input to  
said second digital to analog converter receives data  
from an external wavetable generator.

43. The audio system of Claim 39 wherein an input to  
said second digital to analog converter receives a signal  
comprising mixed wavetable and FM synthesizer data.

44. The audio system of Claim 39 wherein said first  
bitwidth equals said second bitwidth.

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45. The audio system of Claim 39 wherein said first bitwidth is greater than said second bitwidth.

46. The audio system of Claim 39 wherein an input of said first analog to digital converter receives data from an external audio accelerator.

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47. A single chip audio system comprising:

a microcontroller for performing system control operations;

5 a digital to analog converter for converting data selectively received from a bus interface and an accelerator interface;

a mixer for mixing an analog signal output from said digital to analog converter with an analog signal received from a second source;

10 circuitry for idling said mixer when selected signals input to said mixer are muted; and

analog spatial enhancement circuitry for spatially enhancing analog audio data coupled from said mixer operable to:

15 generate a difference signal from first and second signals output from said mixer;

generate an acoustic crosstalk compensation signal from said difference signal;

invert said compensation signal;

20 sum said inverted compensation signal with said first signal; and

sum said compensation signal with said second signal.

25 48. The audio system of Claim 47 wherein said accelerator interface is a serial interface.

49. The audio system of Claim 47 and further comprising a digital signal processor for selectively performing digital processing operations on digital data being input to said digital to analog converters.

30 50. The audio system of Claim 47 wherein said bus interface includes a PNP interface.

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51. The audio system of Claim 49 wherein said digital signal processor performs SRS audio processing functions.

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52. Oscillator start-up circuitry comprising:

a crystal oscillator having buffered and unbuffered outputs;

a hysteresis buffer for generating a output signal  
when an unbuffered clock signal output from said  
unbuffered output falls within a preselected voltage  
range; and

clock-off detection circuitry for monitoring said  
output signal from said hysteresis buffer and controlling  
output of a buffered clock presented at said buffered  
output in response.

53. The circuitry of Claim 52 wherein said hysteresis  
buffer has a center point selected to match a DC bias  
point of said crystal oscillator.

54. The circuitry of Claim 52 wherein said clock-off  
generation circuitry senses a change in logic state of  
said output signal from said buffer within a time-out  
period and generates a clock-on signal in response.

55. The circuitry of Claim 54 wherein output of said  
buffered clock is enabled on a first rising edge of said  
buffered clock after said clock-on signal is asserted.

56. The circuitry of Claim 52 wherein said clock-off  
generation enables output of said buffered clock when  
said unbuffered clock has a large magnitude swing.

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